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1 **Si-emulation: system verification using simulation and emulation**
Zan Yang; Byeong Min; Gwan Choi;
Test Conference, 2000. Proceedings. International , 3-5 Oct. 2000
Pages:160 - 169

[Abstract] [PDF Full-Text (700 KB)] **IEEE CNF**

---

2 **Improving the quality of controls and reducing costs for on-site adjustments with emulation:an example of emulation in baggage handling**
Rengelink, W.; Saanen, Y.A.;
Simulation Conference, 2002. Proceedings of the Winter , Volume: 2 , 8-11 Dec. 2002
Pages:1689 - 1694 vol.2

[Abstract] [PDF Full-Text (446 KB)] **IEEE CNF**

---

3 **Emulation of the Sparcle microprocessor with the MIT Virtual Wires emulation system**
Dahl, M.; Babb, J.; Tessier, R.; Hanono, S.; Hoki, D.; Agarwal, A.;
FPGAs for Custom Computing Machines, 1994. Proceedings. IEEE Workshop on , 10-13 April 1994
Pages:14 - 22

[Abstract] [PDF Full-Text (672 KB)] **IEEE CNF**

---

4 **A Transaction-Based Unified Architecture for Simulation and Emulation**
Hassoun, S.; Kudlugi, M.; Pryor, D.; Selvidge, C.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 13 , Issue: 2 , Feb. 2005
Pages:278 - 287

[Abstract] [PDF Full-Text (456 KB)] **IEEE JNL**

---

5 **A layered adaptive verification platform for simulation, test, and emulation**
Zambaldi, M.; Ecker, W.; Henftling, R.; Bauer, M.;

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---

1 **Predicting error rate for microprocessor-based digital architectures through C.E.U. (Code Emulating Upsets) injection**
Velazco, R.; Rezgui, S.; Ecoffet, R.;
Nuclear Science, IEEE Transactions on , Volume: 47 , Issue: 6 , Dec. 2000
Pages:2405 - 2411

[Abstract] [PDF Full-Text (116 KB)] **IEEE JNL**

---

2 **Using background modes for testing, debugging and emulation of microcontrollers**
Melear, C.;
WESCON/97. Conference Proceedings , 4-6 Nov. 1997
Pages:90 - 97

[Abstract] [PDF Full-Text (444 KB)] **IEEE CNF**

---

3 **Emulation techniques for microcontrollers with internal caches and multiple execution units**
Melear, C.;
WESCON/97. Conference Proceedings , 4-6 Nov. 1997
Pages:544 - 553

[Abstract] [PDF Full-Text (696 KB)] **IEEE CNF**

---

4 **Emulation techniques for microcontrollers**
Melear, C.;
WESCON/97. Conference Proceedings , 4-6 Nov. 1997
Pages:532 - 541

[Abstract] [PDF Full-Text (612 KB)] **IEEE CNF**

---

5 **Using background modes for testing, debugging and emulation of microcontroller**
Melear, C.;
Southcon/95. Conference Record , 7-9 March 1995
Pages:84 - 89

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1 **Validation of the atlas trigger/daq network architecture using hardware data emulators**
LeVine, M.J.; Stancu, S.; Haeberli, C.; Tremblet, L.; Beuran, R.; Meirosu, C.; Dobinson, R.W.; Martin, B.; Knezo, E.; Beck, H.P.; Hauser, R.; Botterill, D.;
Nuclear Science, IEEE Transactions on , Volume: 51 , Issue: 3 , June 2004
Pages:539 - 544

[Abstract] [PDF Full-Text (472 KB)] **IEEE JNL**

---

2 **Configurable multilayer CNN-UM emulator on FPGA**
Nagy, Z.; Szolgay, P.;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on] , Volume: 50 , Issue: 6 , June 2003
Pages:774 - 778

[Abstract] [PDF Full-Text (552 KB)] **IEEE JNL**

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3 **Design of FPGA-based emulator for series multicell converters using co-simulation tools**
Ruelland, R.; Gateau, G.; Meynard, T.A.; Hapiot, J.-C.;
Power Electronics, IEEE Transactions on , Volume: 18 , Issue: 1 , Jan. 2003
Pages:455 - 463

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4 **A novel scheme of implementing high speed AWGN communication channel emulators in FPGAs**
Yongquan Fan; Zilic, Z.;
Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on , Volume: 2 , 23-26 May 2004
Pages:II - 877-80 Vol.2

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---

5 **A fast hardware/software co-verification method for systern-on-a-chip**

by using a C/C++ simulator and FPGA emulator with shared register communication
Nakamura, Y.; Hosokawa, K.; Kuroda, I.; Ko Yoshikawa; Yoshimura, T.;
Design Automation Conference, 2004. Proceedings. 41st , June 7-11, 2004
Pages:299 - 304

[Abstract] [PDF Full-Text (534 KB)] **IEEE CNF**

---

6 **FPGA-based high-speed emulator of quantum computing**
Fujishima, M.;
Field-Programmable Technology (FPT), 2003. Proceedings. 2003 IEEE International Conference on , 15-17 Dec. 2003
Pages:21 - 26

[Abstract] [PDF Full-Text (413 KB)] **IEEE CNF**

---

7 **An embedded in-circuit emulator generator for SOC platform**
Yuan-Long Jeang; Liang-Bi Chen; Yi-Ting Chou; Hsin-Chia Su;
Field-Programmable Technology (FPT), 2003. Proceedings. 2003 IEEE International Conference on , 15-17 Dec. 2003
Pages:315 - 318

[Abstract] [PDF Full-Text (433 KB)] **IEEE CNF**

---

8 **Embedded systems verification with FGPA-enhanced in-circuit emulator**
Meerwein, M.; Baumgartner, C.; Wieja, T.; Glauert, W.;
System Synthesis, 2000. Proceedings. The 13th International Symposium on , 20-22 Sept. 2000
Pages:143 - 148

[Abstract] [PDF Full-Text (448 KB)] **IEEE CNF**

---

9 **Emulator environment based on an FPGA prototyping board**
Kyung-Soo Oh; Sang-Yong Yoon; Soo-Ik Chae;
Rapid System Prototyping, 2000. RSP 2000. Proceedings. 11th International Workshop on , 21-23 June 2000
Pages:72 - 77

[Abstract] [PDF Full-Text (248 KB)] **IEEE CNF**

---

10 **iSAVE: a behavioral emulator for in-system algorithm verification**
Seungjong Lee; Moo-Kyung Jung; In-Cheol Park; Chong-Min Kyung;
ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Conference on , 28-30 Aug. 2000
Pages:303 - 306

[Abstract] [PDF Full-Text (420 KB)] **IEEE CNF**

---

11 **An FPGA-based hardware emulator for fast fault emulation**
Jin-Hua Hong; Shih-Arn Hwang; Cheng-Wen Wu;
Circuits and Systems, 1996., IEEE 39th Midwest symposium on , Volume: 1 , 18-21 Aug. 1996
Pages:345 - 348 vol.1

[Abstract] [PDF Full-Text (392 KB)] **IEEE CNF**

---

12 **A novel approach to real-time verification of transport system design using FPGA based emulator**
Hayashi, K.; Miyazaki, T.; Shirakawa, K.; Yamada, K.; Ichimori, T.; Fukami, K.;

Ohta, N.;
Rapid System Prototyping, 1996. Proceedings., Seventh IEEE International Workshop on , 19-21 June 1996
Pages:5 - 10

[Abstract] [PDF Full-Text (640 KB)] **IEEE CNF**

---

13 **Configurable multi-layer CNN-UM emulator on FPGA**
Nagy, Z.; Szolgay, P.;
Cellular Neural Networks and Their Applications, 2002. (CNNA 2002). Proceedings of the 2002 7th IEEE International Workshop on , 22-24 July 2002
Pages:164 - 171

[Abstract] [PDF Full-Text (401 KB)] **IEEE CNF**

---

14 **Configurable multi-layer CNN-UM emulator on FPGA using distributed arithmetic**
Nagy, Z.; Szolgay, P.;
Electronics, Circuits and Systems, 2002. 9th International Conference on , Volume: 3 , 15-18 Sept. 2002
Pages:1251 - 1254 vol.3

[Abstract] [PDF Full-Text (360 KB)] **IEEE CNF**

---

15 **A hardware accelerator for DSP system design: University of Tehran DSP Hardware Emulator (UTDHE)**
Mahdiany, H.R.; Hormati, A.; Fakhraie, S.M.;
Microelectronics, 2001. ICM 2001 Proceedings. The 13th International Conference on , 29-31 Oct. 2001
Pages:141 - 144

[Abstract] [PDF Full-Text (408 KB)] **IEEE CNF**

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Huisman, L.M.; Daoud, R.;
Test Conference, 1990. Proceedings., International , 10-14 Sept. 1990
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